REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-13. Specifically, the Office Action rejected claims 1 and 4-13 under 35 U.S.C. 102(e), as being anticipated by Chang et al. (U.S. Patent No.6,498,759). The Office Action also rejected claims 2-3 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. Patent No.6,498,759) in view of Applicant's Admitted Prior Art (AAPA) page 2. Claims 1-13 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections Under 35 U.S.C. 102(e)

The Office Action rejected claims 1 and 4-13 under 35 U.S.C. 102(e), as being anticipated by Chang et al. (U.S. Patent No.6,498,759, "**Chang**" hereinafter). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claims 1 and 8 are allowable for at least the reason that the **Chang** does not disclose at least the features of "outputting a voltage adjustment signal **according to the control signal and the system power state signal**", as claimed in claim 1, and "the recognition apparatus outputs a voltage adjustment signal after receiving **the control signal and the system power state signal**", as claimed in claim 8.

Chang disclosed a system for automatic generation of suitable voltage source on motherboard. As shown in FIG. 5 of **Chang**, on starting up a computer system, a power-good signal pulse is provided in step S50. If the power-good signal pulse contains an enable signal, the second voltage is put on the voltage source pin in step S52. Otherwise, control returns to step

S51 where power-good signal pulse is checked again. The CPU reads out the values on the EEPROM of the memory modules in step S53. The type of memory modules inserted to the memory module slot is determined in step S54. If DDR DRAM modules are detected, the second voltage is put on the voltage source pin in step S55. However, if SDRAM modules are detected, the first voltage is put on the voltage source pin in step S56. In the system, the presence of DDR DRAM modules is detected by a general-purpose purpose input/output port through **accessing the recorded data in the EEPROM of the memory module**.

On the contrary, the invention provides a method for automatically determining the type of memory and a motherboard therewith. In the method, the voltage adjustment signal is output **according to the control signal and the system power state signal**, which is used for outputting a configured operation voltage to the memory. When the mode of the computer system changes, for example, the computer system enters a STD mode, a soft off mode, or a mechanical off mode, as shown in the step 360 of Fig.3 of the Specification, the system power state signal enters the low logic state. If the system is in these modes, the recognition apparatus ignores the result of the control signal and directly drives the voltage control circuit to provide the memory module with 2.5V in step 380 of Fig.3.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 8 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4-7 and 9-13 patently define over the prior art as well.

Discussion of Office Action Rejections Under 35 U.S.C. 103(a)

The Office Action also rejected claims 2-3 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. Patent No.6,498,759) in view of Applicant's Admitted Prior Art (AAPA) page 2.

Because the application is filed after November 29, 1999, the cited reference **Chang** and the claimed invention was owned by the same assignee, the reference **Chang** is not qualified as prior art according to the Amendment of Patent Law by the American Inventor Protection Act of 1999 (AIPA), which renders the rejection under 35 U.S.C. 103 moot.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-13 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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